**IN THE CLAIMS:**

1. (Original): A method for providing a metal programmable device, the method comprising:

providing an array of programmable cells;

providing an array of pre-diffused memory cells;

providing a plurality of memory interface control blocks, wherein each memory interface control block accesses the pre-diffused memory cells as a different memory type; and

connecting a first memory interface control block from within the plurality of memory interface control blocks to a first portion of the memory cells, wherein logic within the array of programmable cells accesses at least a first portion of the array of pre-diffused memory cells as a first memory type using the first memory interface control block.

2. (Original): The method of claim 1, wherein the step of connecting the first memory interface control block to the memory cells is performed by applying a metal layer.

3. (Original): The method of claim 1, further comprising:

connecting a second memory interface control block from within the plurality of memory interface control blocks to a second portion of the memory cells, wherein logic within the array of programmable cells accesses at least a second portion of the array of pre-diffused memory cells as a second memory type using the second memory interface control block.

4. (Original): The method of claim 3, wherein the steps of connecting the second memory interface control block to the memory cells is performed by applying a metal layer.

5. (Original): The method of claim 1, wherein the array of pre-diffused memory cells is an array of 6T memory cells.

6. (Original): The method of claim 1, wherein the first memory interface control block and at least one other memory interface control block within the plurality of memory interface control blocks share components.

7. (Original): The method of claim 1, wherein the first memory type is one of a single port random access memory, a dual port random access memory, and a read only memory.

8. (Original): The method of claim 1, further comprising:
programming customer logic by applying a metal layer to the metal programmable device.

9. (Original): A metal programmable device, comprising:
an array of programmable cells;
an array of pre-diffused memory cells; and
a plurality of memory interface control blocks, wherein each memory interface control block accesses the pre-diffused memory cells as a different memory type.

10. (Original): The metal programmable device of claim 9, further comprising:
a metal layer connecting a first memory interface control block from within the plurality of memory interface control blocks to a first portion of the memory cells,
wherein logic within the array of programmable cells accesses the first portion of the memory cells as a first memory type using the first memory interface control block.

11. (Original): The metal programmable device of claim 10, wherein the metal layer connects a second memory interface control block from within the plurality of memory interface control blocks to a second portion of the memory cells and wherein logic within the array of programmable cells accesses at least a second portion of the memory cells as a second memory type using the second memory interface control block.

12. (Original): The metal programmable device of claim 10, wherein the first memory type is one of a single port random access memory, a dual port random access memory, and a read only memory.

13. (Original): The metal programmable device of claim 10, wherein the metal layer programs customer logic within the array of logic programmable cells.

14. (Original): The metal programmable device of claim 10, wherein the metal layer configures at least a portion of the plurality of pre-diffused memory cells.

15. (Original): The metal programmable device of claim 9, wherein the array of pre-diffused memory cells is an array of 6T memory cells.

16. (Original): The metal programmable device of claim 9, wherein the first memory interface control block and at least one other memory interface control block within the plurality of memory interface control blocks share components.

17. (Original): The metal programmable device of claim 9, wherein the plurality of memory interface control blocks are pre-diffused in the metal programmable device.

18. (Original): The metal programmable device of claim 9, wherein each memory interface control block within the plurality of memory interface control blocks has contact points on the surface of the metal programmable device.